SAMSUNG

Samsung and eSilicon Taped Out 14nm Network Processor with Rambus 28G SerDes Solution

*Samsung offers I-Cube™ solution for high-speed interface applications
which will be adopted at AI, Computing, Network and Server applications*

San Jose, USA – Mar. 22, 2017 – Samsung Electronics Co., Ltd., a world leader in advanced semiconductor technology, today announced a successful network processor tape-out based on Samsung's 14LPP (Low-Power Plus) process technology in close collaboration with eSilicon and Rambus. This achievement is built on Samsung's cutting-edge foundry process and design infra for network applications, eSilicon's complex ASIC and 2.5D design capability with its IP solutions, and Rambus' high-speed 28G SerDes solution.

Samsung's 14LPP process technology based on 3D FinFET structure has already been proven for its high performance and manufacturability through mass production track record. The next generation process for network application is 10LPP process which is based on 10LPE (Low-Power Early) of which mass production was started from last year for the first time in the industry. 10LPP process' mass production will be started in this year end.

Additionally, Samsung named its newly developed full 2.5D turnkey solution, which connects a logic chip and HBM2 memory with an interposer, as I-Cube™ (Interposer-Cube) solution. This 14LPP network process chip is the first product that Samsung applied I-Cube™ solution together with Samsung's HBM2 memory. The I-Cube™ solution will be essential to network applications for high-speed signaling, and it is expected to be adopted into other applications such as computing, server and AI in the near future.

"I am delighted to announce 14nm network processor tape-out," said Ryan Lee, Vice President of Foundry Marketing Team at Samsung Electronics. "This successful product tape-out was combined with eSilicon's proven design ability in network area and Rambus' expertise in SerDes and Samsung's robust process technology along with I-Cube solution. This collaboration model is very unique solution which will have very big impact in network foundry segment. Samsung will keep developing its network foundry solution to be a meaningful total network solution provider aligned with its process roadmap from 14nm and 10nm to 7nm."

"This project was a true collaboration between Samsung, Rambus and eSilicon. eSilicon is proud to bring its FinFET ASIC and interposer design skills along with our substantial 2.5D integration skills to the project,'" said Patrick Soheili, Vice President of Product Management and corporate development at eSilicon. "Our HBM Gen2 PHY, custom flip-chip package design and custom memory designs also helped to optimize the power, performance and area for the project."

"Networking OEMs are looking for high-quality leadership IP suppliers that can bring 28G backplane SerDes in advanced FinFET process nodes to market," said Luc Seraphin, senior vice president and general manager of Rambus Memory and Interfaces Division. "Our success with Samsung and eSilicon is a testament that these industry-leading solutions are attainable when you bring leading companies together. This is the first of several other offerings we plan to bring to networking and enterprise ASIC markets around the globe."

*Tape out(T/O): The last step in designing a new chip. By the time of the tape-out, the photo-mask of a chip is completed, and is then ready to be sent to a foundry.

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